

In the Specification:

Please insert the following paragraph on page 1, line 2:

-- This patent arises from a continuation-in-part of US patent application serial number 10/057,493, which was filed on January 24, 2002 and which has issued as U.S. Patent 6,775,748.--

Please amend the paragraph bridging pages 7 and 8 as follows:

-- In addition, one or more of the “hit out” lines are ~~may be~~ connected to a “back-off” input on each processing agent 200. For one embodiment, a first processing agent 200 optionally includes a “back-off” input which is never asserted (e.g., the input is connected to logic zero). This processing agent 200 has the highest priority in an arbitration scheme described in detail below (i.e., no other agent ever tells this agent to “back-off”). A second processing agent 200 may include a “back-off” input which is connected only to the “hit out” of the first processing agent. This processing agent has the second highest priority (i.e., only the highest priority agent can tell this agent to “back-off”). If included in the system, a third processing agent 200 may include a “back-off” input which is connected to the output of a first OR gate 210. The inputs of the first OR gate 210 are in turn connected to the “hit out” signals of the first processing agent 200 and the second processing agent 200. This processing agent has the third highest priority (i.e., either of the highest priority agent and the second highest priority agent can tell this agent to “back-off”). If included in the system, a fourth processing agent 200 may

include a “back-off” input which is connected to the output of a second OR gate 210. The inputs of the second OR gate 210 are in turn connected to the “hit out” signal of the third processing agent 200 and the output of the first OR gate 210. This processing agent 200 has the fourth highest priority (i.e., any of the first three agents can tell this agent to “back-off”). This pattern may continue for any number of processing agents 200 as shown in FIG. 2--

Please amend the paragraph bridging pages 11 and 12 as follows:

-- No other cache 208 currently holds the requested memory block (e.g., no “hit” is generated or a cache directory indicates that no other caches holds the requested block), so main memory 108 supplies the requested block (operation 304). This action requires the memory controller 202 to access the main memory 108 via the system interconnect 106. The cached block is ~~may~~ be tagged “exclusive” to indicate that no other cache 208 currently holds this block (operation 304). --